#11/Response 6.20.03 C Moore

PATENT Attorney Docket No. MTI-31041-A

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Ping, et al.
Serial No.	:	10/046,497
Filing Date	:	October 26, 2001
For	:	Method For Forming Raised Structures by Controlled Selective Epitaxial Growth of Facet Using Spacer
Group Art Unit	:	2814
Examiner	:	LE, Thao X.
Confirmation No.	:	8624

M. Brunson 10/9/03

OK To enter TL 06/26/03

CERTIFICATION UNDER 37 CFR 1.8(a) and 1.10

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RESPONSE AFTER FINAL

Sir:

Applicant requests consideration of the pending Claims 101-116 and 123-223 in the above-identified patent application based on the remarks herein.

Rejections under 35 U.S.C. § 102(e) (Miyano)

The Examiner rejected Claims 101-102, 106-109, 194, and 196-223 under Section 102(e) as anticipated by USP 6,232,641 (Miyano). This rejection is respectfully traversed.

The Examiner cites Miyano as disclosing all of the elements of the claims. The Examiner particularly cites to FIG. 6K of Miyano and the overlying layers 7/12 as being composed of

epitaxial silicon. FIGS. 6A to 6K of Miyano are cross-sectional views of a method of manufacturing an MOS transistor.

Contrary to the Examiner's assertions, Miyano does not teach a device comprised of two overlying layers of epitaxial silicon as claimed by Applicant.

With reference to FIG. 6D, Miyano describes the fabrication of gate electrode 7 as a *polycrystal silicon film* — *not* an epitaxial silicon film, which is deposited by CVD and etched (at col. 8, lines 39-52, emphasis added):

> Then, as shown in FIG. 6D, a gate oxide film 6 having a thickness of about several nm is formed by thermal oxidation. Then, *a gate electrode 7 made of polycrystal silicon* is formed on the gate oxide film 6. The selected longitudinal direction of the gate electrode 7 is the direction <110> of the silicon substrate 1.
>
> A specific method of forming the gate electrode 7 will now be described. That is, a *polycrystal silicon film* which has a thickness of 200 nm and which will be formed into the gate electrode 7 *is deposited on the gate oxide film 6 by a CVD method* or the like. *Then, a photoresist pattern is formed on the polycrystal silicon film which is used as a mask in a process for etching the polycrystal silicon film. Thus, the gate electrode 7 is formed.*

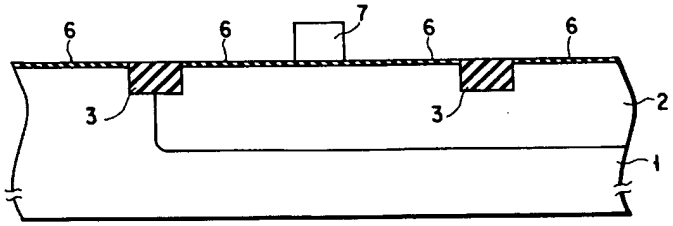

FIG. 6D

Then — referring to FIG. 6I — Miyano describes forming layer 12 as an *epitaxial silicon film* (at col. 10, lines 51-56; emphasis added):

> Then, as shown in FIG. 6I, *a vapor phase epitaxial growth method is employed to form an epitaxial silicon film (a single crystal silicon film) 12* having a thickness of about 50 nm on the source diffusion layer 8 and the drain diffusion layer 9 allowed to appear after the SiO_2 liner 10 and the gate oxide film 6 have been removed.

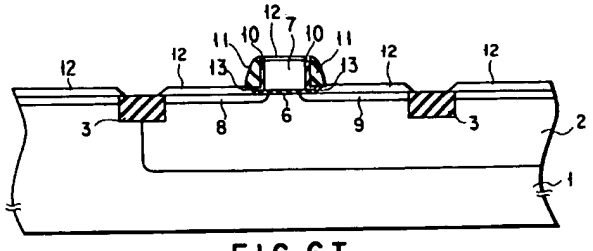

FIG. 6I

Thus, Miyano distinguishes the two layers 7/12 — the gate electrode layer 7 being a *polycrystal silicon* film — and layer 12 being an *epitaxial silicon* film.

Miyano does not teach or suggest a structure comprising at least two overlying layers of epitaxial silicon as claimed by Applicant. Accordingly, withdrawal of this rejection is respectfully requested.

Rejections under 35 U.S.C. §103(a)

The Examiner rejected Claims 101-116, 123-130, 132-135, 137-160 and 165-223 under Section 103(a) as obvious over USP 5,397,909 (Moslehi) in view of USP 5,902,125 (Wu). The Examiner rejected Claim 131 as obvious over Moslehi in view of USP 5,963,822 (Saihara). The Examiner also rejected Claims 103-104 and 110 as obvious over Miyano in view of USP 6,051,473 (Ishida). These rejections are respectfully traversed.

No argument regarding to SSG/SEG

Moslehi combined with Wu. With regard to the rejection of Claims 101-116, 123-130, 132-135, 137-160 and 165-223, the Examiner cites Moslehi as disclosing all of the elements of the claims (citing to FIG. 19) — except for the uppermost epitaxial silicon layer having an insulated top surface. However, the Examiner asserts that it would be obvious to apply an insulator on the top surface of the epitaxial layer of Moslehi's device based on the disclosure in Wu (citing to FIG. 8).

FIGS. 15 through 19 of Moslehi illustrate a structure for interconnecting a transistor to a remote device. Referring to FIG. 18, after formation of the source/drain junction regions 92 and the upper gate region 94, Moslehi *blanket deposits a refractory metal layer 97* over the semiconductor layers 92, 94.

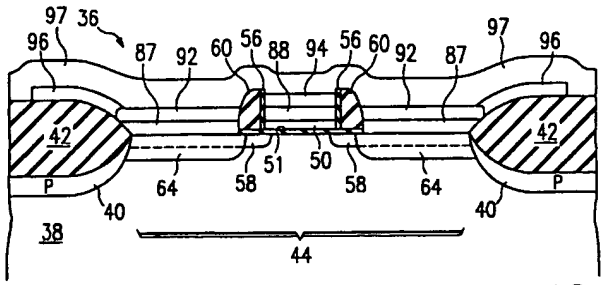

FIG. 18

Then, as shown in FIG. 19, Moslehi reacts the refractory metal layer 97 with the semiconductor layers 92, 94 to form metal interconnect segments 98, 100.

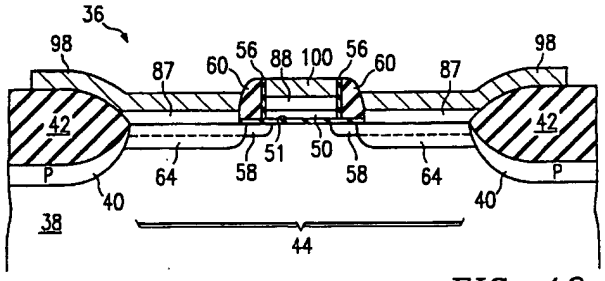

FIG. 19

Moslehi emphasizes the advantage to forming local interconnects according to that process at col. 20, lines 60-66:

> From the above, it may be appreciated that the present invention provides a novel and practical process and structure involving the construction and interconnection of a transistor device...Additionally, the novel interconnect scheme provided in accordance with the present invention permits the formation of local interconnects utilizing reacted refractory metals with semiconductor underlayers and therefore eliminates the need for using refractory metal nitrides or high electrical resistance interconnects.

Wu teaches depositing an oxide layer 26 *to isolate* the gate structure. Contact holes 28 generated through the oxide layer are then refilled with a conductive material layer 30 (see, col. 5, lines 15-19; emphasis added):

> Referring to FIG. 7, *a thick oxide layer 26 is formed over the substrate 2 and gate structure for isolation*. For example, CVD oxide can be used for in this step. Then, contact holes 28 are generated in the oxide layer 26 and aligned to the source and drain 22 by using conventional manner.

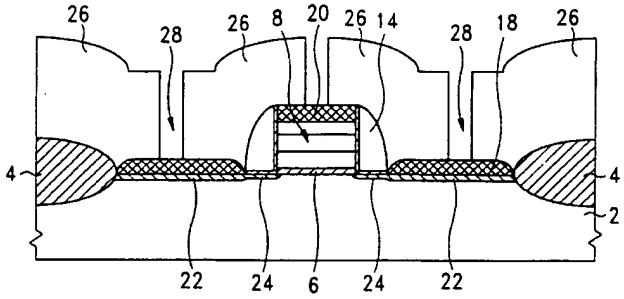

FIG.7

The deposit of an oxide layer that would isolate the semiconductor layers 92, 94 of Moslehi's structure would be contrary to Moslehi's process for forming metal interconnect segments 98, 100. Moslehi explicitly teaches depositing a refractory metal layer 97 over semiconductor layers 92, 94, and then *reacting layers* 97 and 92, 94 to form metal interconnect segments 98, 100.

Contrary to the Examiner's assertion, one skilled in the art reading Moslehi would *not* be motivated to deposit an insulating layer over the uppermost epitaxial silicon layer of Moslehi's structure. Accordingly, withdrawal of the rejection of the claims based on the combination of Moslehi with Wu is respectfully requested.

Moslehi combined with Saihara. The Examiner rejected Claim 131 as obvious over Moslehi in combination with Saihara.

Claim 131 depends from Claim 129, and is directed to a structure comprising at least two overlying layers of epitaxial silicon — *each* silicon layer having a top surface defining a facet having a (100) plane orientation — and the uppermost epitaxial layer having an insulated top surface.

The Examiner maintains that Claim 131 is made obvious based on Saihara to form an epitaxial layer of Moslehi's structure having a (100) facet.

First of all, Saihara describes methods for forming a *single* epitaxial film layer on a surface of a (100) silicon substrate - not two overlying epitaxial layers.

Second, as admitted by the Examiner, Moslehi does not teach or suggest an uppermost epitaxial layer having an insulated top surface. Further, as discussed above, the deposit of an oxide layer over the semiconductor layers 92, 94 of Moslehi's structure would be contrary to Moslehi's process for forming metal interconnect segments 98, 100 — by reacting a deposited refractory metal layer 97 with semiconductor layers 92, 94.

Combining the teaching of Saihara with that of Moslehi would not arrive at Applicant's structure as recited in Claim 131. Accordingly, withdrawal of this rejection of the claims is respectfully requested.

Miyano combined with Ishida. Finally, the Examiner rejected Claims 103-104 and 110 as obvious over Miyano in combination with Ishida.

The Examiner cites Ishida (FIG. 2) for disclosing S/D regions comprising at least two overlying layers of epitaxial silicon 250, 260. The Examiner maintains that it would be obvious to combine the S/D regions of Ishida with the structure of Miyano.

Ishida essentially *teaches away* from the fabrication of a S/D made of raised epitaxial layers. In describing prior art structures, Ishida — at col. 2, lines 25-57, emphasizes the *drawbacks* of fabricating raised S/D MOSFET's by selective epitaxial growth including the difficulties in (i) selectively growing the raised epitaxial layers 250, 260 (FIG. 2), (ii) maintaining shallow S/D regions 240 due to dopant diffusion during the heat cycles in the epi layer formation, and (iii) maintaining a sufficiently thick sidewall oxide layer 270 along the gate when subjected to the cycles required for epitaxy. See also at col. 4, lines 5-57, again discussing the disadvantages to selective epitaxial growth to form a raised source-drain MOSFET.

Ishida re-emphasizes the drawbacks of selective epitaxial growth to form S/D regions in the Description of the invention (at col. 4, line 58 to col. 5, line 4; emphasis added):

> Because selective epitaxial growth of layers 350 and 360 is difficult, and because the various heat steps, including those occurring during epi growth and silicide formation, cause diffusion of source and drain regions 340, the method described with reference to FIGS. 3A-3F is *considered impractical*.
>
> Thus, in accordance with the invention, a method of forming a raised drain-source MOSFET is disclosed which avoids many of the above-discussed difficulties and which is described with reference to FIGS. 4A-4E...

Thus, Ishida essentially *teaches away* from forming a S/D of epitaxial silicon layers.

Based on the teachings of Ishida, there is no motivation to alter Moslehi's structure with a raised S/D comprising overlying epitaxial layers.

Furthermore, as discussed above, Miyano does not teach a device comprised of two overlying layers of epitaxial silicon. Again, as illustrated in FIGS. 6D and 6I (see above), Miyano fabricates the gate electrode 7 as a *polycrystal silicon film* — *not* as an epitaxial silicon film, and fabricates layer 12 as an epitaxial silicon film. See Miyano at col. 8, lines 9-52, and col. 10, lines 51-56. Miyano does not teach or suggest a transistor gate structure comprising at least two overlying layers of epitaxial silicon.

Therefore, even if, *arguendo*, one were to combine the teaching of Ishida with Miyano, it would not provide Applicant's structures as claimed. Accordingly, withdrawal of this rejection of the claims is respectfully requested.

Information Disclosure Statement. Enclosed herewith is a Supplemental Information Disclosure Statement and Form 1449/PTO listing references submitted in a corresponding divisional application USSN 10/379,494, with a check for the required fee.

Consideration of the listed references is requested.

Extension of Term. The proceedings herein are for a patent application and the provisions of 37 CFR § 1.136 apply. Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that Applicant has inadvertently overlooked the need for a petition for extension of time. If any extension and/or fee are required, please charge Account No. 23-2053.

Based on the above remarks, the Examiner is respectfully requested to reconsider and withdraw the rejections of the claims. It is submitted that the present claims are in condition for allowance, and notification to that effect is respectfully requested.

Respectfully submitted,

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Dated: June 6, 2003

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